INTEL CONFIDENTIAL
Attorney-Client Privileged Communication

TMG INVENTION DISCLOSURE
Located at: http://legal.intel.com

LEGAL ID# _____(legal dept. use only) DATE: _____
It is important to provide accurate and detailed information on this form (fill in ALL areas under Inventor[s]). The information will be used to evaluate your invention for possible filing as a patent application. When completed, please return this form to **Intel Legal Department at JF3-147. You can submit electronically via e-mail to "invention disclosure submission" if all of the information is electronic, including drawings and supervisor approval.** If you have any questions regarding this form or to whom it should be forwarded, please call

Fill out the below and follow the instructions:

1. **Field of the Invention:**
   - ☐ Semiconductor Process: device and integration
   - ☐ Semiconductor Process + Equipment: thin films
   - ☐ Semiconductor Process + Equipment: etch/litho
   - ☐ Circuit Design
   - ☐ Flash
   - ☐ Test
   - ☐ CQN (Q&R)
   - √ Packaging
     - ☐ Boards/Cartridge
     - ☐ Automation
   - ☐ Other

2. **Concise Title of Invention:** The process of making electrically conductive structures of flip-chip packages by using fluxing underfill materials

3. Brief Description of Invention (please use only space provided and font #10 or larger. Write the Key Elements of the Invention):

The invention is: a novel process of making electrically conductive structures for fine pitch flip-chip packages by using fluxing no-flow underfill materials. With the help of instant chip joint machine, this process is invented to provide simultaneous chip joint and underfill by using filled or non-filled fluxing underfill materials (no-flow underfill materials). Therefore, the new process can significantly simplify the flip-chip package manufacturing process and reduce manufacturing cycle time and cost.

The key elements are: instant chip joint process powered by fluxing underfill materials.

4. Inventor(s):

Name: Carlos A. Gonzalez
E-Mail Address: WWID# M/S:

Phone: Fax: Home Address:

Citizenship: Supervisor Name: Supervisor Phone: Supervisor M/S:

Group Name: TMG Contractor: Inventor Signature:
Division Name: ATD_X_
PTD___ CTM___ CR___ YES _____
STTD___ CQN ___
SMTD____TCAD___ NO ____X____
Other?_____

Name: Song-Hua Shi

E-Mail Address: WWID# M/S:

Phone: Fax: Home Address:

Citizenship: Supervisor Name: Supervisor Phone: Supervisor M/S:

Group Name: TMG Contractor: Inventor Signature:
Division Name: ATD___
PTD___ CTM___ CR___ YES _____
STTD___ CQN ___
SMTD____TCAD___ NO _____
Other?_MTO_____

Name: Milan Djukic

E-Mail Address: WWID# M/S:

Phone: Fax: Home Address:

Citizenship: Supervisor Name: Supervisor Phone: Supervisor M/S:

Group Name: TMG Contractor: Inventor Signature:
Division Name: ATD___
PTD___ CTM___ CR___ YES _____
STTD___ CQN ___
SMTD____TCAD___ NO _____
Other?_____

(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

5. HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM (use first inventor's supervisor if multiple inventors)

DATE: _____ SUPERVISOR NAME: _____

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID.

6. Has subject matter of present disclosure been disclosed or will it be disclosed outside Intel?
If yes, explain and give date: No
(Give expected tape out date if applicable):

7. Has the subject matter of present disclosure been published or will it be published outside of Intel? No
If yes, explain and give date:

8. Has a product using or manufactured using the present disclosure been sold or offered for sale?
If yes, explain and give date: No

9. Has this invention been conceived, or constructed during accomplishment of a government or third party contract? If yes, give contract name and number: No

10. Explain the problem being addressed by the invention:

This invention addresses the problem of: a) low assembly yield by using silica filled no-flow underfill material, b) low reliability by using non-filled no-flow underfill materials, c) complexity and throughput time of current capillary flow underfill d) assembly cost

11. Explain current state of the art (i.e, how the problem is solved today):

Today, we cannot make use of no-flow technology for CPU packages because non-filled materials do not meet the CTE and modulus requirements to make a reliable package. On the other hand, filled no-flow materials (new formulations driven by Intel) cannot be used with the current pick&place and reflow process.

12. Explain technical advantages of the invention over current state of the art:

The technical advantage of this invention is: the use of silica-filled no-flow underfill materials and low CTE no-flow underfill materials is allowed in this invented process with satisfactory interconnection yield. The interconnection yield is significantly improved due to the low viscosity and fluxing capability of the liquid no-flow underfill material. Moreover, the instant chip join machine can provide reasonably high chip placement force to effectively increase the contact opportunity of bump to pad during chip join process, and therefore further effectively improve the interconnection yield.

13. a. **Is the invention experimentally verified? Yes**
    b. **Is the invention verified with simulation?**
    c. **If neither a. or b. above, then you can get a patent on the concept, but please explain the technical basis to justify that your invention will work (use extra space if necessary):**

The experimental data will be provided by [redacted]
Include x-section images here

The technical basis are as follows:
The fluxing capability in the no-flow underfill materials can effectively remove the metal oxide on the surface of bumps, pads, pre-solders, and copper columns during the soaking period at temperature ranging from 130°C to 180°C to allow good wetting of the substrate solder material to die bump (copper or high lead). The high placement force and low viscosity of the no-flow materials can effectively increase the contact opportunity between bump and pad and facilitate the squeezing out of silica particles in between the bumps and bump-shaped pre-solder pads during solder wetting process. As a result, the interconnection yield is significantly improved. Since the no-flow underfill is heavily silica-filled or low CTE no-flow material, the satisfactory reliability of the assembled packages are also achieved.

14. **Detailed Description of Invention (try to use only the space provided with font #10 or larger type. Refer to your drawings):**

The uniqueness of this invention is the use of liquid silica-filled fluxing no-flow underfill materials or low CTE fluxing no-flow underfill materials. The fluxing capability in the no-flow underfill materials can effectively remove the metal oxide on the surface of bumps, pads, pre-solders, and copper columns during the soaking period at temperature ranging from 130°C to 180°C to allow the quick wetting of solder material to copper and high lead material. The high placement force and low viscosity of the no-flow materials can effectively increase the contact opportunity between bump and pad and facilitate the squeezing out of silica particles in between the bumps and bump-shaped pre-solder pads during solder wetting process. As a result, the interconnection yield is significantly improved. Since the no-flow underfill is heavily silica-filled or low CTE no-flow material, the satisfactory reliability of the assembled packages are also achieved.

In this process (Figure 2), the silica-filled no-flow underfill material or low CTE underfill material is dispensed at the center of bonding pad area on a pre-heated substrate. A chip is then picked-up and heated to soaking temperature, aligned and compressed down to the underfill material. After the chip reaches the position, it is held for sometime (soaking time) to allow the flux to remove the metal oxide. Then, the chip is heated above the melting temperature of the solder while maintaining the placement force. After that, the entire structure is cooled down naturally and may experience post-cure if needed.

Referenced sketches/dwg's/diagrams: (use additional page(s))

15.

Drawings (use as many pages as needed)
(PLEASE DO NOT MAKE COLOR DRAWINGS)

Figure 1. Present State of the Art (often this is helpful to explain your invention, but it is not required).

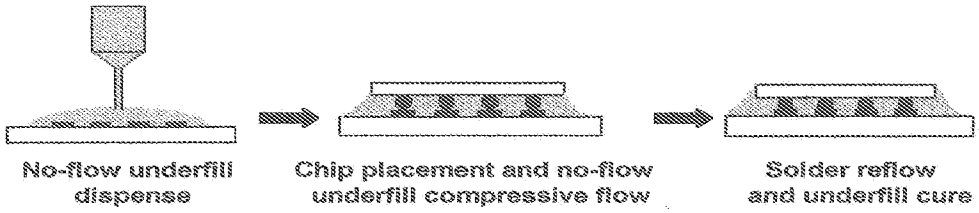


Figure 1 (a): No-flow underfill process

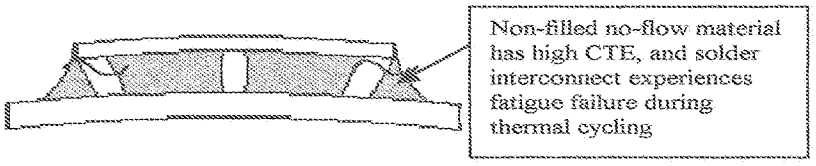


Figure 1 (b): Non-filled no-flow underfill material can not effectively protect solder interconnects

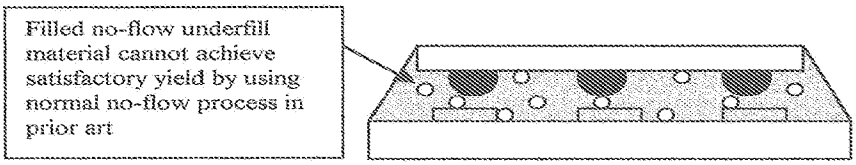
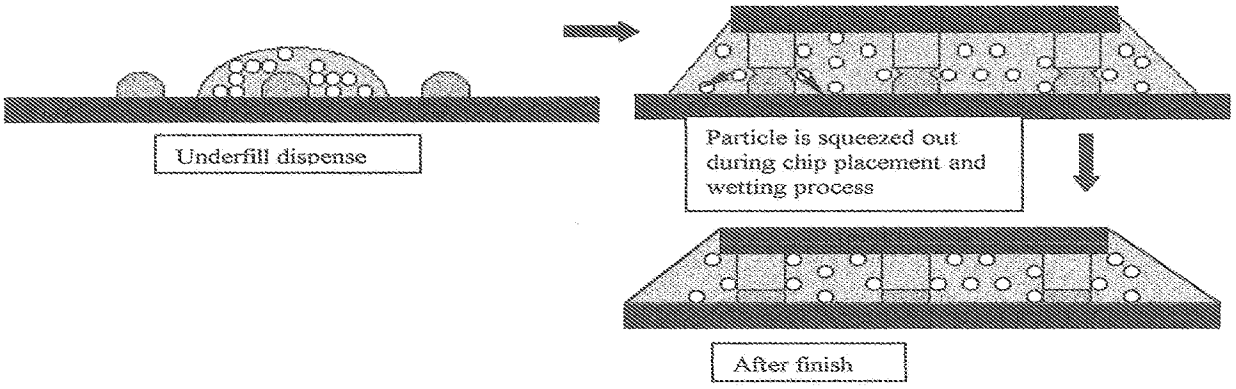


Figure 1 (c): Filled no-flow material significantly reduce interconnection yield by silica inclusion in-between the bump and bonding pad.

Figure 2. The invention (use additional figures as needed to show details and additional embodiments)



16. Key Supporting Data (1 page limit on separate page):

    Will be provided by [redacted]

17. What is the product or process invention to be used on? (e.g., P8xx, name of product, etc.):
    P1262 and X64 products

18. Have you reviewed your invention with a TMG Patent Mentor? (see below for mentor names) If so, give name: _____

19. Any other information IP committee should consider? No